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(54) SEMICONDUCTOR DEVICE

HALBLEITERANORDNUNG

DISPOSITIF A SEMI-CONDUCTEURS

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(56) References cited:
JP-A- 0 567 463
JP-A-49 128 684
JP-A-59 143 359
JP-A-59 144 168
US-A- 4 497 043

- **PATENT ABSTRACTS OF JAPAN, vol. 8, no. 107 (E-245)[1544], 19th May 1984; & JP-A-59 22 359 (NIPPON DENKI K.K.) 04-02-1984**
- **IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-31, no. 1, January 1984, pages 89-95, IEEE, New York, US; S. KRISHNA et al.: "An analog technology integrates bipolar, CMOS, and high-voltage DMOS transistors"**
- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 16, no. 8, January 1974, pages 2701- 2703, New York, US; I. ANTIPOV: "Forming complementary field-effect devices and NPN transistors"**

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EP 0 245 515 B1

forth in the further claims.

In the present invention, a voltage which is still negative (in general, when a p-type silicon substrate is used) or positive (in general, when an n-type silicon substrate is used) with respect to the operating voltage of circuitry is applied to a portion liable to the injection of minority carriers, for example, a substrate.

Further, in the present invention, in order to solve problems ascribable to the method of applying the voltage as stated above, for example, the problem that voltages to be applied to individual devices increase to degrade the reliability of a device of low breakdown voltage such as a microminiature device, the isolation region of MOS transistors of identical conductivity type or bipolar transistors of identical conductivity type is divided into several isolated regions, to which suitable isolation voltages are applied according to the respective uses.

Brief Description of the Drawings:

Fig. 1 is a sectional view showing a prior art, Fig. 2 is a sectional view showing an embodiment of the present invention, Fig. 3 is a sectional view showing an embodiment of a CMOS structure, Fig. 4 is a sectional view showing an embodiment of a bipolar structure, Fig. 5 is a sectional view showing an embodiment of a bipolar-CMOS complex structure, Fig. 6 is a sectional view showing an embodiment of an SOI structure, Fig. 7 is a block diagram of a memory, Fig. 8 is a diagram showing an embodiment for the application of a substrate isolation voltage to a memory, Figs. 9 - 11 are sectional views each showing an embodiment of a MOS dynamic memory, Figs. 12 and 13 are sectional views each showing an embodiment of a bipolar-CMOS complex dynamic memory, Fig. 14 illustrates sectional views showing an embodiment of principal steps for realizing the structure in Fig. 13, Fig. 15 is a sectional view showing another embodiment of the bipolar-CMOS complex dynamic memory, Fig. 16 is a plan view with the embodiment of Fig. 15 seen from the front surface of a chip, and Fig. 17 illustrates sectional views showing an embodiment of principal steps for realizing the structure in Fig. 16.

Best Mode for Carrying Out the Invention:

Now, the details of the present invention will be described in conjunction with embodiments.

Fig. 2 illustrates an integrated circuit of nMOS transistors. A construction in the figure is such that a p-type substrate (p-Sub) is formed therein with an n-well layer NW, in which p-well layers PW_1 and PW_2 are further formed. The nMOS transistors formed in the two p-wells and the substrate p-Sub are respectively denoted by symbols nMOS1, nMOS2 and nMOS3. In this structure, voltages V_{BB1}, V_{BB2} and V_{BB3} independent of one another can be applied to the isolation layers of the three sorts of nMOS transistors, and they can be selected at suitable voltages according to circuit uses.

On the other hand, the supply voltage V_{CC} or a voltage which is at least higher than both the voltages V_{BB2} and V_{BB3} is applied as V_{BB4} to the n-well layer NW. Although the single nMOS transistor has been shown in Fig. 2, one well usually has a plurality of nMOS transistors in each of three isolation layers.

In addition, although the two p-wells and the single n-well have been shown in Fig. 2, this embodiment is also applicable to a combination wherein a plurality of n-wells are provided and wherein one or more p-wells are designed in each of the n-wells. Further, the present invention can be readily applied to a pMOS integrated circuit merely by altering the conductivity types of the substrate, wells and MOS transistors and reversing all the potential relations. The voltage V_{BB1} may be applied to the substrate either from the front surface or from the rear surface thereof.

Fig. 3 illustrates an embodiment in which the present invention is applied to a CMOS (complementary MOS) structure. Referring to the figure, three n-wells (NW_1, NW_2, NW_3) are formed in a p-type substrate, and p-wells (PW_1, PW_2) are further formed in the respective n-wells NW_1 and NW_2. Thereafter, nMOS transistors (nMOS1, nMOS2, nMOS3) are respectively formed in the p-wells (PW_1, PW_2) and the substrate p-Sub. Besides, pMOS transistors (pMOS1, pMOS2, pMOS3) are respectively formed in the n-wells (NW_1, NW_2, NW_3). In this construction, voltages V_{BB2}, V_{BB4} and V_{BB1} are applied to the p-type isolation layers for the nMOS transistors. On the other hand, voltages V_{BB3}, V_{BB5} and V_{BB6} are applied to the n-type isolation layers for the pMOS transistors. As three voltages V_{BB2}, V_{BB4} and V_{BB1} or as three voltages V_{BB3}, V_{BB5} and V_{BB6}, voltages of at least two values unequal to each other are applied according to circuits used. By way of example, voltages of GND (0 V) and -3 V are applied as the voltages V_{BB2}, V_{BB4} and V_{BB1}, while voltages of V_{CC} (+5 V) and $V_{CC} + \alpha$ (+7 V) are applied as the voltages V_{BB3}, V_{BB5} and V_{BB6}. In this way, the voltages as desired can be applied to the individual isolation layers of the nMOS and pMOS transistors. Although, in Fig. 3, only one MOS transistor has been shown in each of the wells, a plurality of MOS transistors may well be provided as are necessary. In addition, although the numbers of the wells are 3 as the n-wells and 2 as the p-wells in Fig. 3, they may be increased or decreased as are necessary. Further, it is to be understood that the present invention is also applicable to a construction wherein the polarities of the substrate and the wells are inverted. That is to say, p-wells are first formed in an n-type substrate and wherein n-wells are subsequently formed.

While the embodiments described above concern the construction employing only the MOS transistors, there will now be described examples in each of which the present invention is applied to an integrated circuit employing bipolar transistors or an integrated circuit having both bipolar and MOS transistors.

Fig. 4 illustrates an embodiment in which the

pacitances between the collectors of bipolar transistors and the substrate) can be reduced, and an impurity concentration profile less prone to soft errors can be selected for the cell array. By the way, the designations of isolation voltages for use in the following embodiments shall correspond to the symbols V_{BBM1}, V_{BBM2}, V_{BBM3} and V_{BBM4} in Fig. 8 in accordance with the roles thereof.

Sectional views of embodiments of chips which are obtained for the embodiment of the chip setup in Figs. 7 and 8 will be elucidated below. Each of them illustrates the sectional structure of the portions of the input circuit and dynamic memory cell of a MOS dynamic RAM in correspondence with the prior-art example in Fig. 1. Although the memory cell is the dynamic cell here, the present invention is similarly applicable to a MOS static memory cell and a bipolar static memory cell.

In an embodiment in Fig. 9, the nMOS transistors of an input protection circuit (an n-type diffused resistor and an nMOS diode) and an input circuit are formed in a p-well (pW), the pMOS transistor of the input circuit is formed in an n-well (nW), and a memory cell made of an nMOS transistor is formed in a p-type substrate p-Sub. In the present embodiment, the p-well of the input circuit and the substrate p-Sub are isolated. Therefore, the values of the isolation voltages V_{BBM2} and V_{BBM4} of the respective regions can be independently set. Accordingly, by way of example, the voltage V_{BBM2} can be selected at -3 V in order to satisfy the specifications of the input circuit, and the voltage V_{BBM4} can be selected at 0 V from the viewpoint of the soft-error immunity of the memory cell. A broken line under the memory cell indicates a p-type high impurity concentration layer. In this way, the disadvantage of the prior-art example elucidated in Fig. 1 can be prevented to provide a stable dynamic memory.

In Fig. 10, only the n-type diffused resistor and nMOS diode of an input protection circuit are provided in a p-well, and the nMOS transistors of any other peripheral circuits are formed in a p-type substrate p-Sub likewise to a memory cell. Besides, a pMOS transistor can be formed in an n-well. A voltage V_{BBM2} (for example, -3 V) is applied to the p-well under the n-type diffused resistor and nMOS diode which are input protection devices, while a voltage V_{BBM4} (for example, 0 V) is applied to the substrate p-Sub of the nMOS transistors of the input circuit and the memory cell. A p-type high concentration layer is provided under the memory cell as in Fig. 9. A voltage V_{BBM1} is applied to the n-well. The present embodiment is advantageous over the embodiment of Fig. 9 in that, since only the input protection devices are provided in the well, the layout is simplified, and that, since the nMOS transistors other than the input protection diode are formed under the same concentration condition over the cell and the peripheral circuit, the control of threshold voltages V_{TH} is easy.

Fig. 11 illustrates an embodiment in which a memory cell is formed in a p-well (pW), while the nMOS transistors of an input protection circuit and any other peripheral circuit are formed in a p-type substrate p-Sub. In the present embodiment, the p-well of comparatively high concentration is provided under the memory cell, and it acts as the substitute of the high concentration layer indicated by the broken line in Fig. 9 or 10.

In the above embodiments are applied to the MOS memories (SRAM, DRAM). Next, embodiments in each of which the present invention is applied to a memory by the use of the BiCMOS construction of Fig. 5 having both bipolar and MOS devices will be described with reference to Figs. 12 - 16. Among the embodiments, those of Figs. 12 - 14 employ epitaxial layers, and those of Figs. 15 - 17 don't employ epitaxial layers.

Fig. 12 shows the nMOS, pMOS and n-p-n bipolar transistors of peripheral circuits, and a dynamic type nMOS memory cell as viewed from the left.

Under the nMOS memory cell, a p-type buried layer (pBL) of high impurity concentration is put to intensify the soft-error immunity. This layer pBL is also used for the isolation of an n-type buried layer.

Although the nMOS transistor of the peripheral circuit is formed in a p-well, this p-well can be omitted when a p-type epitaxial layer is employed. An n-type buried layer nBL of high concentration is provided under this p-well layer, and an n-layer (CN) of high concentration is added for feeding a voltage to the layer nBL. Besides, the p-well has its side surrounded with an n-well thereby to be isolated from a p-type substrate p-Sub. A voltage V_{BBM2} (for example, -3 V) is applied to the nMOS transistor of the peripheral circuit, and the voltage V_{BBM1} (for example, a supply voltage V_{CC}) to the n-well of the pMOS transistor. A common voltage V_{BBM4} is applied to the isolation layer of the n-p-n bipolar transistor and that of the nMOS transistor of the memory cell. Buried layers nBL and pBL provided under a well serve to reduce the collector resistance of the bipolar transistor, and are also effective to prevent latch-up through the decrease of a substrate resistance.

Fig. 13 illustrates an embodiment in which a memory cell is formed in a p-type substrate p-Sub, and the difference of which from the embodiment of Fig. 12 consists only in a construction under the memory cell. With the construction in Fig. 12, the buried layer pBL of high concentration might rise and cause the threshold voltage V_{TH} of the nMOS transistor to fluctuate. In contrast, according to the construction in Fig. 13, a p-type high concentration layer indicated by a broken line is provided only under a storage capacitor so as to prevent the buried layer from rising to the channel part of the nMOS transistor of the memory cell.

Next, principal steps for realizing the sectional structure of Fig. 13 are illustrated in Fig. 14. At (a) in Fig. 14, n-type buried layers nBL are formed in the front surface of a p-type substrate, and at (b), a p-type buried layer pBL is further formed. Thereafter, a layer Epi is formed by epitaxial growth at (c), and n-wells (nWELL) and p-wells (pWELL) are formed in the layer Epi by steps (d) and (e). At (f), layers CN heavily doped with

source and drain of said first conductivity type (p) is formed in said third well layer (nW3) at its surface and
the value of a fourth voltage (VBB6) applied to said third well layer (nW3) is different from that of said first voltage.

4. A semiconductor device formed within a first region of a substrate (p-Sub) of a first conductivity type (p) comprising

a first well layer (nW) of the second conductivity type (n) formed within said first region, a second well layer (pW1, pW2) of the first conductivity type (p) formed within said first well layer (nW), a first bipolar transistor npn3) having a first emitter and a first collector of said second conductivity type (n) and a first base of said first conductivity type (p), a second bipolar transistor (npn1, npn2) having a second emitter and a second collector of said second conductivity type (n) and a second base of said first conductivity type (p), wherein said first bipolar transistor (npn3) is formed in said first region at its surface and said second bipolar transistor (npn1, npn2) is formed in said second well layer (pW1, pW2) at its surface, wherein said first base is disposed in said first collector and wherein said first emitter is disposed in said first base, wherein said second base is disposed in said second collector and wherein said second emitter is disposed in said second base,
first voltage means to apply a first voltage (VBB4) to said first well layer (nW), second voltage means to apply a second voltage (VBB2, VBB3) to said second well layer (pW1, pW2) and third voltage means to apply a third voltage (VBB1) to said first region,
wherein the first voltage (VBB4) isolates the second well layer (pW1, pW2) and said first region,
and wherein the value of said second voltage (VBB2, VBB3) is different from that of said third voltage (VBB1).

5. The semiconductor device according to claim 4, wherein a third bipolar transistor (pnp1) of the second type (pnp) having emitter and collector of said first conductivity type (p) and a base of said second conductivity type (n) is formed in the first well layer (nW) at its surface.

6. The semiconductor device according to any of claims 1 to 5, wherein said first conductivity type is p-type and said second conductivity type is n-type.

Patentansprüche

1. Halbleiterbauelement, das in einem ersten Bereich eines Substrat (p-Sub) eines ersten Leitungstyps (p) ausgebildet ist, mit

einer ersten Wannenschicht (nW) des zweiten Leitungstyps (n), die in dem ersten Bereich ausgebildet ist, einer zweiten Wannenschicht (pW1, pW2) des ersten Leitungstyps (p), die in der ersten Wannenschicht (nW) ausgebildet ist,
einem ersten Feldeffekttransistor mit einem isolierten Gate (nMOS3) eines ersten Kanal-Typs mit einer Source und einem Drain des zweiten Leitungstyps (n), der im ersten Bereich an dessen Oberfläche ausgebildet ist, und einem zweiten Feldeffekttransistor mit einem isolierten Gate (nMOS1, nMOS2) des ersten Kanal-Typs mit einer Source und einem Drain des zweiten Leitungstyps (n), der in der zweiten Wannenschicht (pW1, pW2) an deren Oberfläche ausgebildet ist,
einer ersten Spannungseinrichtung zum Anlegen einer ersten Spannung (VBB4) an die erste Wannenschicht (nW), einer zweiten Spannungseinrichtung zum Anlegen einer zweiten Spannung (VBB2, VBB3) an die zweite Wannenschicht (pW1, pW2) und einer dritten Spannungseinrichtung zum Anlegen einer dritten Spannung (VBB1) an den ersten Bereich,
wobei die erste Spannung (VBB4) die zweite Wannenschicht (pW1, pW2) und den ersten Bereich isoliert, und
wobei der Wert der zweiten Spannung (VBB2, VBB3) von dem der dritten Spannung (VBB1) verschieden ist.

2. Halbleiterbauelement gemäß Anspruch 1, wobei ein dritter Feldeffekttransistor mit einem isolierten Gate (pMOS1, pMOS2) des zweiten Kanal-Typs mit einer Source und einem Drain des ersten Leitungstyps (p) in der ersten Wannenschicht (nW1, nW2) an deren Oberfläche ausgebildet ist.

3. Halbleiterbauelement gemäß einem der Ansprüche 1 oder 2, wobei eine dritte Wannenschicht (nW3) des zweiten Leitungstyps (n) im ersten Bereich ausgebildet ist,

ein vierter Feldeffekttransistor mit einem isolierten Gate (pMOS3) des zweiten Kanal-Typs mit einer Source und einem Drain des ersten Leitungstyps (p) in der dritten Wannenschicht (nW3) an deren Oberfläche ausgebildet ist, und der Wert einer an die dritte Wannenschicht (nW3) angelegten vierten Spannung (VBB6) von dem der ersten Spannung verschieden ist.

4. Dispositif à semiconducteurs formé dans une première région d'un substrat (p-Sub) d'un premier type (p) de conductivité, comprenant

une première couche formant puits (nW) du second type (n) de conductivité formée dans ladite première région, une seconde couche formant puits (pW1, pW2) du premier type (p) de conductivité formée dans ladite première couche formant puits (nW),
un premier transistor bipolaire (npn3) ayant un premier émetteur et un premier collecteur dudit second type (n) de conductivité et une première base dudit premier type (p) de conductivité, un second transistor bipolaire (npn1, npn2) ayant un second émetteur et un second collecteur dudit second type (n) de conductivité et une seconde base dudit premier type (p) de conductivité, ledit premier transistor bipolaire (npn3) étant formé dans ladite première région sur sa surface et ledit second transistor bipolaire (npnl, npn2) étant formé dans ladite seconde couche formant puits (pW1, pW2) sur sa surface, ladite première base étant disposée dans ledit premier collecteur et ledit premier émetteur étant disposé dans ladite première base, ladite seconde base étant disposée dans ledit second collecteur et ledit second émetteur étant disposé dans ladite seconde base,
un premier moyen d'application de tension pour appliquer une première tension (VBB4) à ladite première couche formant puits (nW), un second moyen d'application de tension pour appliquer une seconde tension (VBB2, VBB3) à ladite seconde couche formant puits (pW1, pW2) et un troisième moyen d'application de tension pour appliquer une troisième tension (VBB1) à ladite première région,
la première tension (VBB4) étant isolée de la seconde couche formant puits (pW1, pW2) et de ladite première région,
et la valeur de ladite seconde tension (VBB2, VBB3) étant différente de celle de ladite troisième tension (VBB1).

5. Dispositif à semiconducteurs selon la revendication 4, dans lequel un troisième transistor bipolaire (pnp1) du second type (pnp) ayant un émetteur et un collecteur dudit premier type (p) de conductivité et une base dudit second type (n) de conductivité est formé dans la première couche formant caisson (nW) sur sa surface.

6. Dispositif à semiconducteurs selon l'une quelconque des revendications 1 à 5, dans lequel ledit premier type de conductivité est le type p et ledit second type de conductivité est le type n.

FIG. 3

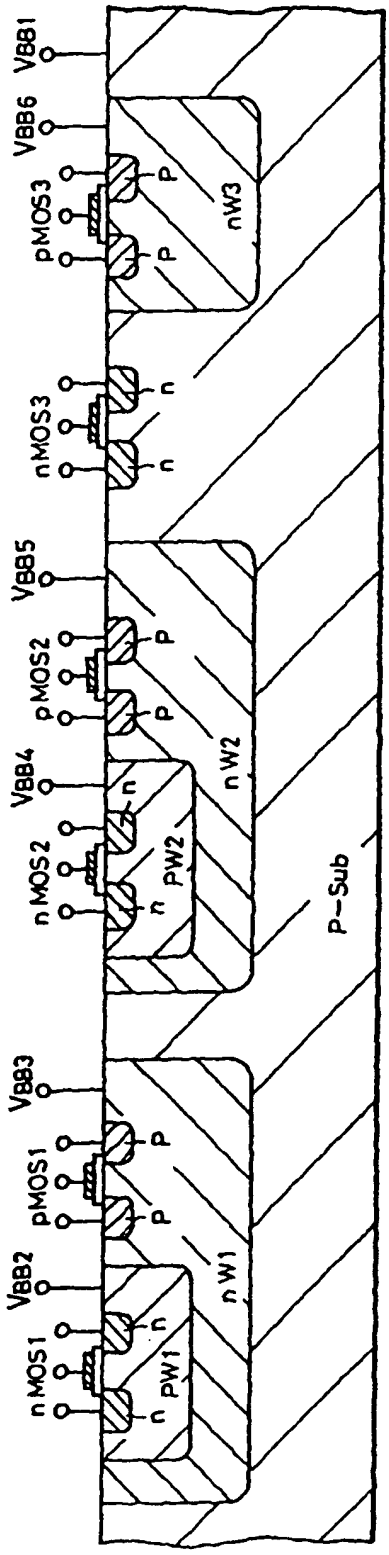

VBB1
VBB6
pMOS3
P
P
nW3
nMOS3
n
n
VBB5
pMOS2
P
P
nW2
VBB4
n
nMOS2
n
PW2
P-Sub
VBB3
pMOS1
P
P
nW1
VBB2
n
nMOS1
n
PW1

FIG. 6

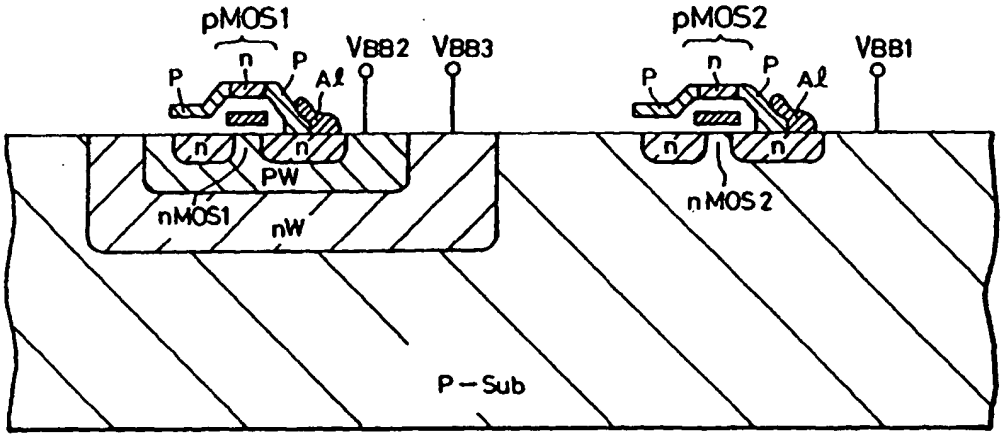


FIG. 9

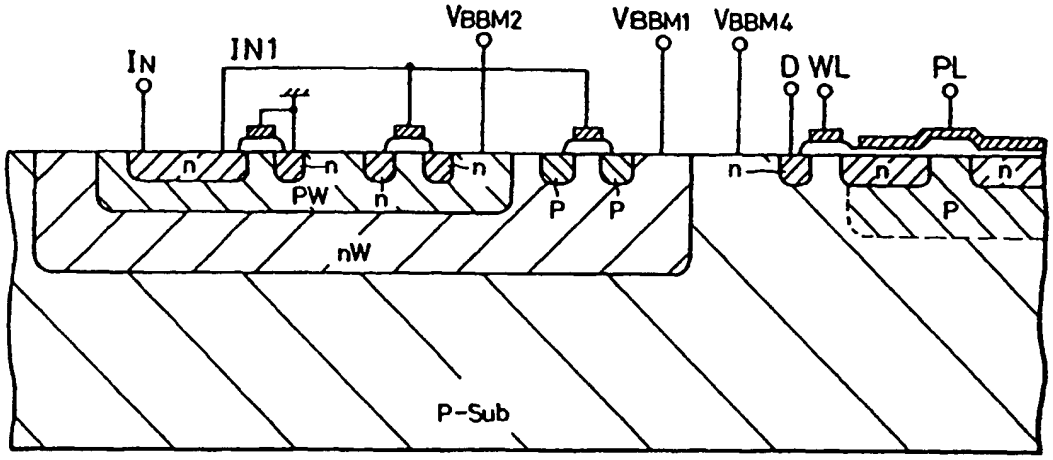


FIG. 10

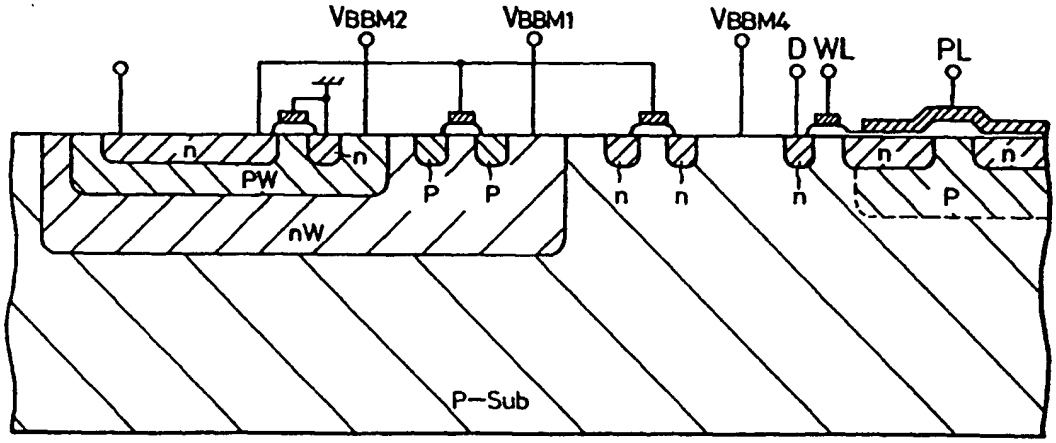


FIG. 11

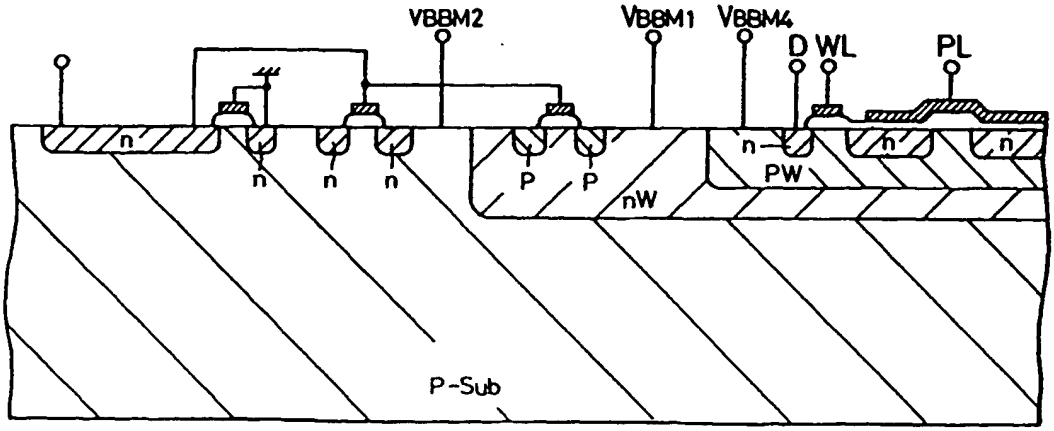
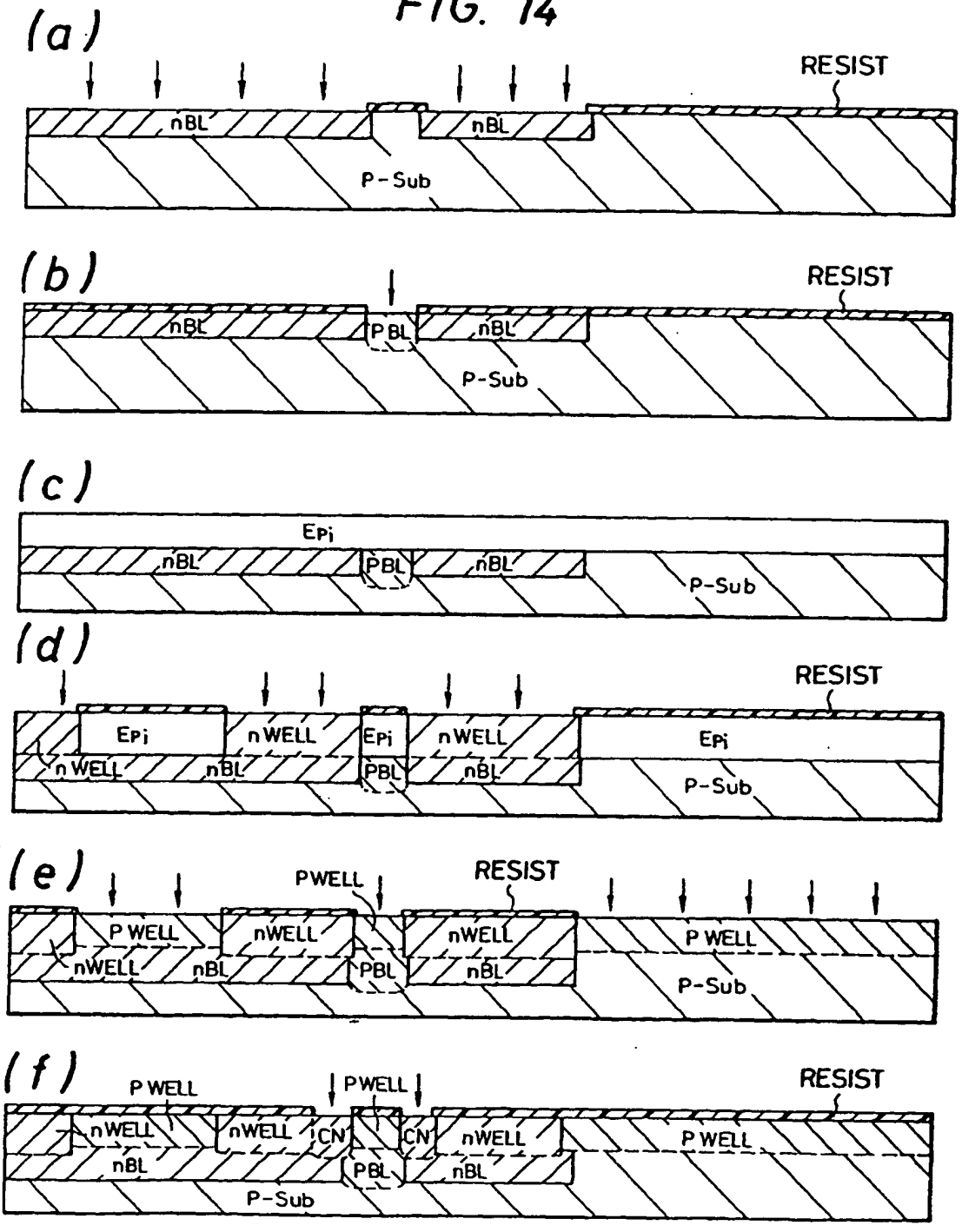


FIG. 14


(a)
RESIST
nBL
nBL
P-Sub
(b)
RESIST
nBL
PBL
nBL
P-Sub
(c)
Epi
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PBL
nBL
P-Sub
(d)
RESIST
Epi
nWELL
Epi
nWELL
Epi
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nBL
P-Sub
(e)
PWELL
RESIST
P WELL
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nWELL
P WELL
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nBL
PBL
nBL
P-Sub
(f)
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PWELL
RESIST
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CN
CN
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P WELL
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PBL
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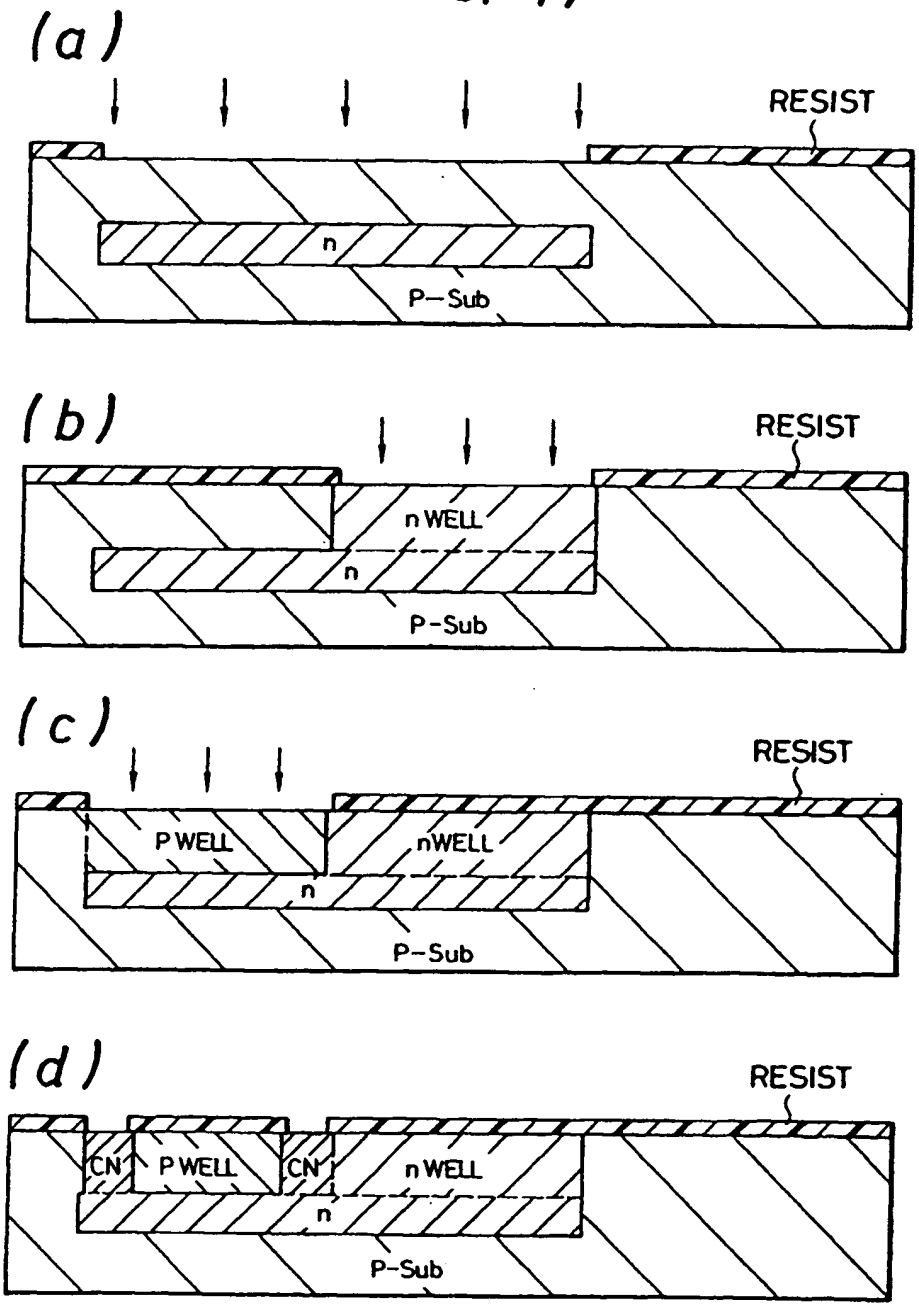
P-Sub

FIG. 17


(a)
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n
P-Sub
(b)
RESIST
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(c)
RESIST
P WELL
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(d)
RESIST
CN
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CN
n WELL
n
P-Sub